Local charge transport in nanoscale amorphous and crystalline regions of high-*k* $(Zr0_2)_{0.8}(Al_2O_3)_{0.2}$ thin films

Dominik Martin,[1,a)] Matthias Grube,[1] Walter M. Weber,[1] Jürgen Rüstig,[1] Oliver Bierwagen,[2] Lutz Geelhaar,[3] and Henning Riechert[3]
[1]*Namlab gGmbH, 01187 Dresden, Germany*
[2]*Department of Materials, University of California, Santa Barbara, California 93106-5050, USA*
[3]*Paul-Drude-Institut für Festkörperelektronik, 10117 Berlin, Germany*

(Received 24 June 2009; accepted 16 September 2009; published online 6 October 2009)

The charge transport in $(Zr0_2)_{0.8}(Al_2O_3)_{0.2}$ thin films consisting of nanoscale crystallites in an amorphous matrix were investigated by conductive atomic force microscopy. Local current-voltage curves were obtained either from multiple current images for different biases or by ramping the tip bias at a specific location. Comparison of both approaches for amorphous matrix sites implies that they are equivalent. Current-voltage curves for crystallite and amorphous sites are different, but repeated voltage ramps at amorphous sites yield curves as obtained at pristine crystallites. This suggests charge transport through leakage paths along defects at grain boundaries and along stress-induced defects at amorphous sites. © *2009 American Institute of Physics*.
[doi:10.1063/1.3243987]

Very high dielectric constant insulator materials as required for future memory and logic technology nodes are very difficult to achieve with purely amorphous thin films since high dielectric constants are only obtained in crystalline phases. Epitaxial layers would be challenging to implement in conventional Si technology, but the three-dimensional geometry and high aspect ratio for dynamic random access memory (DRAM) capacitors exclude this approach entirely. Accordingly, the dielectric must be in a nano- or polycrystalline phase, but these layers are prone to significantly higher leakage currents. For materials that are inhomogeneous on the nanoscale, these are highly local effects. Conventional macroscopic measurements integrate over a fairly large area and cannot spatially resolve nanoscale properties such as individual grains. Thus, charge transport should be studied on the nanoscale, e.g., with conductive atomic-force microscopy (CAFM). A comparison between morphology and current mappings yields already valuable information.

We recently observed that in $(Zr0_2)_{0.8}(Al_2O_3)_{0.2}$ thin-film leakage takes place at crystallites in an otherwise amorphous matrix.[1] In order to elucidate the actual transport mechanisms, current-voltage curves (*I-V* curves) have to be acquired with high spatial resolution. However, the unambiguous association of an entire *I-V* curve with a nm-sized location presents a considerable experimental challenge. Here, we study the charge carrier transport behavior at crystallites and at amorphous sites in $(Zr0_2)_{0.8}(Al_2O_3)_{0.2}$ thin films by extracting local *I-V* curves from current maps acquired at different voltages. Thus, sample regions that are structurally completely different but only tens of nanometer apart are investigated almost simultaneously. The validity of this approach is assessed by the comparison with conventional *I-V* curves taken while the AFM tip was at rest above a matrix site.

The dielectric $(Zr0_2)_{0.8}(Al_2O_3)_{0.2}$ film studied is 20 nm thick and was grown by molecular beam deposition at 500 °C on a highly *n*-doped Si substrate with 4-nm-thin TiN on top. A Veeco DI-3100 AFM equipped with a TUNA-Module preamplifier was used for local electrical characterization. Electrically conductive platinum-coated tips were used to form a local metal-insulator-metal structure along with the TiN bottom electrode and the high-*k* dielectric. Two kinds of measuring strategies were used. Conventional *I-V* curves were measured by ramping the bias voltage up and down at a specific AFM-tip location on the film. The sweep rate was 1 V/s. To avoid anionic oxidation, the tip was grounded and the substrate was set on negative bias. Before measurement the experimental setup was given enough time for thermal stabilization in order to reduce thermal drift and ensuring the *I-V* curve to be truly taken at the defined location. This approach was used to examine amorphous matrix sites by ramping the bias voltages from 0 to 9.0 V and back to 0 V.

As confirmed by transmission electron microscopy and grazing incidence x-ray diffractometry the hillocks in the morphology mappings correspond to crystallites, some of which extend from the TiN through the entire dielectric layer.[1] To examine the leakage spot evolution of hillock sites a different approach was followed. Since leakage currents are a highly localized transport mechanism it should be ensured that the *I-V*-curves are taken precisely at a hillock site by avoiding piezo-scanner effects like "creep" and "warp." This was achieved by taking a series of simultaneous morphology and current maps of the same area at discrete bias voltages. The bias voltage was changed consecutively from image to image, from 0 to 4.0 V and back to 0 V again. Such a series is partially presented in Fig. 1. Figures 2(b) and 2(c) show *I-V* curves that are assigned to each location by taking into account the entire set of current maps. This is similar to the technique of Seko *et al.*[3] and Nikiforov *et al.*[4] but this work considers a much larger amount of images, up to 90, enabling a significantly more detailed analysis. There is a basic difference between the two approaches. In the first case the voltage was ramped while the tip was at rest at a specific location, while in the second case the voltage was main-

a)Electronic mail: dominik.martin@namlab.com.

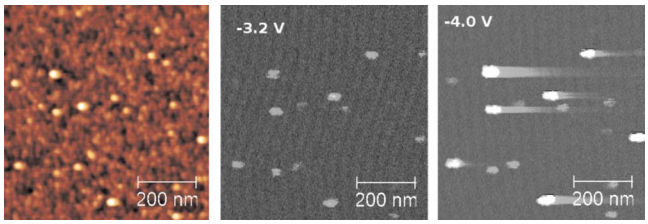

FIG. 1. (Color online) Part of a bias voltage series: Left: Morphology mapping, false color scale is 3 nm. Center: Current mapping of the same area at 3.2 V, color scale is 53.50 pA [nonlinear (Ref. 2)]. Right: Current mapping at 4.0 V, color scale is 100 pA (nonlinear). The morphology does not change during the entire bias series. The striping artifacts are a capacitance effect induced by the preamplifier.

tained constant while the tip was scanning. To compare this method with *I-V* curves taken at specific locations, the latter approach was performed for amorphous matrix sites as well [Fig. 2(b)].

The case of leakage current in the amorphous matrix is discussed first and then compared to the leakage current evolution at crystallite sites. In the following discussion the bias voltage where the measured absolute current exceeds 10 pA is named v_c when bias is increased and v_c' when the bias is decreased. Figure 2 a shows *I-V* curves taken at a site in the amorphous matrix and starting at 0 V, here v_c is $6.8\ \mathrm{V} \pm 0.3\ \mathrm{V}$ (averaged over three matrix sites). The increase of current is fairly consistent with Fowler–Nordheim conduction. At 100 pA the maximum measureable current is reached. As the bias voltage is decreased again v_c' is $6.4\ \mathrm{V} \pm 0.2\ \mathrm{V}$. The hysteresis, i.e., the difference between v_c and v_c', is small $(0.4 \pm 0.1\ \mathrm{V})$. For the later comparison with crystallites it will be important to know how the *I-V* curves develop when the same site in the amorphous matrix is repeatedly stressed. In this case the leakage behavior changes as generally observed in CAFM measurements.[5–8] In later ramps v_c' is shifted to values between $3.0 \pm 1\ \mathrm{V}$ and v_c to $5.0 \pm 1\ \mathrm{V}$ and hysteresis is significantly larger than before. Here v_c and v_c' vary so much that taking an average of different locations and measurements does not contribute to clarity. To demonstrate *I-V* characteristics the 104th ramp is shown in Fig. 2(a). It is noticeable that currents are larger at low bias, and the hysteresis is increased. Figure 2(b) shows *I-V* curves taken at amorphous sites by extraction from current mappings. These show the same behavior as the first voltage ramps on a fixed location. This is crucial for the interpretation of the *I-V* curves extracted for the crystallite sites, at which conventional *I-V* curves cannot be measured reliably. Comparison of Fig. 2(a) and 2(b) suggests that both types of *I-V* measurement yield equivalent results, which is an important finding for the value of CAFM in general.

In contrast, Fig. 2(c) shows the *I-V* curves extracted for pristine crystallite sites, which exhibit a different behavior. Here, v_c is $3.2 \pm 0.2\ \mathrm{V}$ and v_c' is $1.4 \pm 0.1\ \mathrm{V}$, resulting in a mean hysteresis of $1.8 \pm 0.3\ \mathrm{V}$ (averaged over five hillock sites).

Literature agrees that conduction in ZrO_2 occurs through defect states within the electronic band gap. These defects are assumed to be oxygen vacancies and/or oxygen interstitials in the amorphous matrix and at grain boundaries.[5,9–12] These defects act as traps and as a stepping stone for the formation of filamentary leakage current paths according to the percolation model.[13,14] Figure 3 schematically depicts the formation of such a leakage path. Initially, defect density is not sufficiently high across the entire dielectric layer from the TiN to the AFM tip to allow a current to flow [Fig. 3(a)]. As a consequence, the local electric field varies [note the different electric fields in Fig. 3(b)] across the dielectric. In the region where the leakage path was formed the net field is lowered due to the injected electrons. Since the externally applied voltage is the same, the net field where the leakage path has not been established is stronger. At high bias voltage a current is measured. Additional oxygen vacancies are created due to high current and high electrical fields[7,15,16] [Fig. 3(c)]. This process eventually leads to a local soft breakdown[17,18] at high voltage when a critical trap density is reached. It has to be emphasized that defect-assisted conduction is not well understood and that for a complete description different types of defects and many mesoscopic processes such as anion migration would have to be taken into consideration.

Our results suggest the following processes. In the amorphous matrix, a filamentary leakage path develops as the bias voltage exceeds a certain v_c, and as the bias is decreased again the leakage path is still present leading to a v_c' lower than v_c. In successive *I-V* ramps the electrical stress induces more and more defects, and thus v_c and v_c' are lowered. Figure 3(b) shows how in addition to enabling a filamentary leakage path by trap hopping, defects may also be charged during the *I-V* measurement, increasing v_c. Figure 3(b) also depicts how these defects act as traps for tunneling electrons. Consequently, an internal electrical field, contrary to the applied bias, forms resulting in a higher v_c. In Fig. 3(c) bias voltage is sufficiently high to detrap charge carriers at these sites. These defect states are now transient positions for charge carriers giving a significant rise to current. As bias is decreased again trapping becomes more efficient when bias voltage is sufficiently low. This bias voltage v_c' is much lower than v_c, resulting in a large hysteresis [Fig. 3(d)]. Such

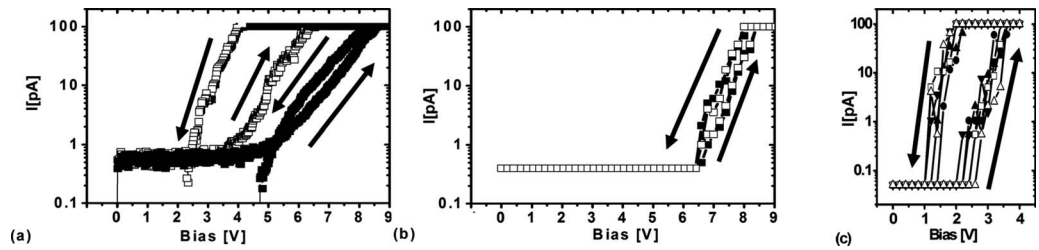

FIG. 2. (a) Local *I-V* curves acquired in the amorphous matrix by ramping the current while the tip rests on a specific location. Solid squares show the first ramp and open squares the 104th ramp where a filamentary leakage path is already formed. The *I-V*-curves were started at 0 V. (b) Local *I-V* curves acquired in the amorphous matrix by extracting the current from an image series. Different symbols represent different locations. (c) Local *I-V* curves acquired on crystallites by extracting the current from an image series. Different symbols represent different locations.

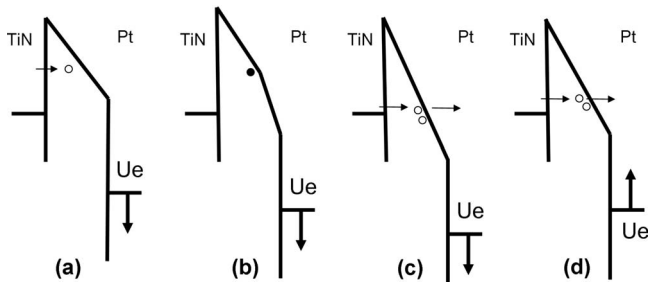

FIG. 3. (a) Schematic energy band diagram of tunneling into unoccupied defect state (empty circle) in dielectric layer at low bias voltage U. (b) Contrary internal field induced by trapped charge (full circle) in the dielectric layer. (c) Conduction via trap states by tunneling into them and detrapping when bias is sufficiently large. (d) Conduction via trap states by tunneling into them and detrapping as bias is decreased.

a large hysteresis is generally associated with charging, as in Fig. 2 a for the 104th ramp.[17,19] The size of the hysteresis depends on the amount of charge that may be trapped in the dielectric layer at low bias since this determines the strength of the contrary internal field.

For crystallite sites it is known that oxygen vacancies and interstitials are a common defect at grain boundaries.[9,10] Thus, the leakage path is already present prior to measurement. This explains the large hysteresis at pristine sites in Fig. 2(c). The injected charge carries are trapped at low bias voltage and then detrapped at high bias voltage resulting in a high v_c. When bias voltage is decreased again trapping surpasses trap assisted conduction only at low bias voltages v_c' (Fig. 3(d)). The fact that the morphology remains unchanged during the entire series and the shape of the decreasing I-V curve is retained confirms that no hard breakdown took place.[20]

The comparison of the measurements made at crystallite sites and at amorphous sites reveals remarkable similarities for repeatedly stressed matrix sites and previously unstressed crystallite sites. In both cases, the hysteresis is significantly larger than for unstressed matrix sites and absolute v_c and v_c' are much lower. This is consistent if we bear in mind that electrical stress activates traps which form the leakage path in the amorphous matrix,[16] thus creating a situation similar to defects along a grain boundary across the entire layer. Moreover, the shape of the I-V curves [Figs. 2(a) and 2(c)] is for both types of sites irregular and different from the exponential increase observed for the unstressed matrix [Figs. 2(a) and 2(b)]. While the latter is typical for the Fowler–Nordheim dominated conduction, the irregular shape suggests that trap-assisted charge carrier transport mechanisms dominate conduction in unstressed crystallite and prestressed amorphous sites. Li *et al.*[16] and Lucovsky *et al.*[9] reported on higher leakage current at broken down amorphous sites in an oxygen deficient leakage path, and at oxygen vacancies at crystal grain boundaries respectively. Together with our observations this suggests a similarity of defect types but different defect densities at both locations. The different absolute values of v_c and v_c' in crystallite and amorphous sites is determined by the defect density and the number of defects acting as traps. These defects are more likely to form along the grain boundary than inside the crystallites. Therefore, the current voltage measurements confirm our earlier tentative observation that leakage takes place preferably at the boundaries of crystallites and not through the grains.[1]

In conclusion, local I-V curves extracted from series of CAFM current mappings at different biases are equivalent to local I-V measurements acquired with the CAFM tip at rest. Sites in the amorphous matrix and at crystallites show clearly different local I-V curves, while electrically pre-stressed matrix sites exhibit the same behavior as crystallites. These data can be explained by filamentary leakage paths that form either along existing defects at grain boundaries or along stress-induced defects in the amorphous matrix.

The authors are grateful to Infineon Technologies AG for access to their CAFM laboratory and for fruitful discussions with Johannes Heitmann, Stefan Jakschik, Thomas Mikolajick, and Gunther Jegert. This work was supported by the German Federal Ministry of Education and Research (BMBF) under the MEGAEPOS project.

[1] O. Bierwagen, L. Geelhaar, X. Gay, M. Piesins, B. Jobst, A. Rucki, and H. Riechert, Appl. Phys. Lett. **90**, 232901 (2007).
[2] http://gwyddion.net
[3] A. Seko, T. Sago, M. Sakashita, A. Sakai, M. Ogawa, and S. Zaima, Jpn. J. Appl. Phys., Part 1 **45**, 2954 (2006).
[4] M. N. Nikiforov, M. J. Brukman, and D. A. Bonnell, Appl. Phys. Lett. **93**, 182101 (2008).
[5] S. Kremmer, H. Wurmbauer, G. Tallarida, S. Spiga, C. Wiemer, M. Fanciulli, and C. Teichert, J. Appl. Phys. **97**, 074315 (2005).
[6] L. Aguilera, M. Porti, M. Nafria, and X. Aymerich, IEEE Electron Device Lett. **27**, 157 (2006).
[7] J. Petry, W. Vandervorst, L. Pantisano, and R. Degraeve, Microelectron. Reliab. **45**, 815 (2005).
[8] W. Weinreich, L. Wilde, M. Lemberger, V. Yanev, M. Rommel, E. Erben, J. Heitmann, U. Schröder, L. Oberbeck, A. J. Bauer, and P. Kücher, J. Vac. Sci. Technol. B **27**, 364 (2009).
[9] G. Lucovsky, C. C. Fulton, Y. Zhang, Y. Zou, J. Luning, L. F. Edge, J. L. Whitten, R.J. Nemanich, H. Ade, D. G. Schlom, V. V. Afanase'v, A. Stesmans, S. Zollner, D. Triyoso, and B. R. Rogers, IEEE Trans. Device Mater. Reliab. **5**, 65 (2005).
[10] G. Lucovsky, D. M. Fleetwood, S. Lee, R. D. Schrimpf, J. A. Felix, J. Jüling, M. Ulrich, and D. E. Aspnes, IEEE Trans. Nucl. Sci. **53**, 3644 (2006).
[11] J. Robertson, K. Xiong, and B. Falabretti, IEEE Trans. Device Mater. Reliab. **5**, 84, (2005).
[12] H. Park, M. Jo, H. Choi, M. Hasan, R. Choi, P. D. Kirsch, B. H. Lee, T.-W. Kim, T. Lee, and H. Hwang, IEEE Electron Device Lett. **29**, 54 (2008).
[13] Y. Okuyama, S. Kamohara, Y. Manabe, K. Okuyama, K. Kubota, T. Kobayashi, and K. Kimra, Tech. Dig. - Int. Electron Devices Meet. **1998**, 905.
[14] R. Degraeve, G. Groeseneken, R. Bellens, J. L. Ogier, M. Depas, P. J. Roussel, and H. E. Maes, IEEE Trans. Electron Devices **45**, 904 (1998).
[15] R. Waser and M. Aono, Nature Mater. **6**, 833 (2007).
[16] X. Li, C. H. Tung, and K. L. Pey, Appl. Phys. Lett. **93**, 262902 (2008).
[17] M. Houssa, T. Nigam, P. W. Mertens, and M. M. Heyns, Appl. Phys. Lett. **73**, 514 (1998).
[18] E. Miranda, J. Sune, R. Rodriguez, M. Nafria, F. Martin, and X. Aymerich, Jpn. J. Appl. Phys., Part 1 **38**, 2223 (1999).
[19] R. Agaiby, P. Hofmann, D. Zhou, M. Kerber, J. Heitmann, U. Schroeder, E. Erben, and L. Oberbeck, IEEE Electron Device Lett. **30**, 340 (2009).
[20] S. Lombardo, J. H. Stathis, K. L. Pey, F. Palumbo, C. H. Tung, and P. Linder, J. Appl. Phys. **98**, 121301, (2005).