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Electrical performance of phase change memory cells with $\text{Ge}_3\text{Sb}_2\text{Te}_6$ deposited by molecular beam epitaxy

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Here, we report on the electrical characterization of phase change memory cells containing a $\text{Ge}_3\text{Sb}_2\text{Te}_6$ (GST) alloy grown in its crystalline form by Molecular Beam Epitaxy (MBE). It is found that the high temperature growth on the amorphous substrate results in a polycrystalline film exhibiting a rough surface with a grain size of approximately 80–150 nm. A detailed electrical characterization has been performed, including I-V characteristic curves, programming curves, set operation performance, crystallization activation at low temperature, and resistance drift, in order to determine the material related parameters. The results indicate very good alignment of the electrical parameters with the current state-of-the-art GST, deposited by physical vapor deposition. Such alignment enables a possible employment of the MBE deposition technique for chalcogenide materials in the phase change memory technology, thus leading to future studies of as-deposited crystalline chalcogenides as integrated in electrical vehicles. © 2015 AIP Publishing LLC.

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Phase Change Memory (PCM) is a Non-Volatile Memory (NVM) technology that relies on the capability of making reversible transitions between the crystalline and amorphous phases of chalcogenide materials, such as $\text{GeTe-Sb}_2\text{Te}_3$ (GST) alloys, exploiting the large electrical resistance contrast between these two phases.^{1–3} It has been shown that this technology has good scaling capabilities^{1,3} and good lifetime cycle performance.⁴ Such properties, combined with the fast read and write speed, make the PCM technology very attractive for partially replacing existing memory technologies or for new applications, like the Storage Class Memory (SCM), filling both the access time and the cycle lifetime gap between storage and memory applications.^{1,3}

The GST layers of studied memory elements as found in the literature are typically grown by sputtering at 180–190 °C (Physical Vapor Deposition, PVD), resulting in partially amorphous layers that are subsequently annealed in order to be crystallized. Other deposition techniques are, for example, Chemical Vapor Deposition (CVD), in the 300–400 °C range⁵ and Atomic Layer Deposition (ALD), below 100 °C,⁶ both reported as suitable techniques for GeSbTe alloys deposition. Recently, it has been shown that crystalline phase change multi-layers can have improved functional properties,⁷ indicating that the crystalline growth of phase change materials is a viable approach for device fabrication. Molecular Beam Epitaxy (MBE) is a well established deposition method and has been successfully used to fabricate epitaxial phase change materials, making advanced studies on the properties of these materials possible.⁸ For example, it was shown that the crystalline orientation of phase change materials before and after an amorphization-recrystallization cycle remains the same.⁹ Furthermore, GST films grown by MBE were used to provide evidence for topological band inversion in GST alloys.¹⁰ Besides its ability to grow epitaxial thin films, MBE also offers a high degree of material purity and control of the

deposition rates of individual elements. These aspects make this technique attractive for studying the effects of doping, change of composition, and for the deposition of super-lattice structures. However, a necessary step in the evaluation of the potential of conventional phase change materials grown by MBE appears to be their characterization in terms of electrical behavior on an evaluation vehicle.

Here, we report on the deposition of a $\text{Ge}_3\text{Sb}_2\text{Te}_6$ alloy in memory device structures using MBE. Instead of performing the GST deposition in the range of 180–190 °C, the chalcogenide material is deposited at 250 °C, here resulting in as-deposited poly-crystalline films. The detailed electrical characterization shows that the fabricated memory elements have good switching characteristics and all the material-related parameters that can be collected from the electrical tests are shown to be in very good agreement with those taken from state-of-the-art PVD GST.

In order to allow for electrical characterization of the MBE grown material, a dedicated vehicle containing metal plugs with a 2500 nm² contact area was used as a substrate for chalcogenide film deposition. The vehicle only contains amorphous materials on the surface. The substrates were chemically and physically cleaned, loaded in the load-lock of the MBE system, and heated to 150 °C for 30 min for out-gassing. Subsequently, they were transferred into a second chamber where another out-gassing was performed, this time at 350 °C for 30 min. Afterwards, the samples were transferred to the deposition chamber (base pressure: 2×10^{-10} mbar) and heated to the deposition temperature of 250 °C. For the deposition, dual-filament effusion cells were used containing Ge, Sb, and Te and a 2:3:5 flux ratio was employed. The duration of the deposition was 240 min and the deposited GST films have a thickness of approximately 70 nm. Based on the XRD data of epitaxial films grown on $\text{Si}(111)-(\sqrt{3} \times \sqrt{3})\text{-Sb}$ under the same conditions, the

composition of the films is estimated to be $\text{Ge}_3\text{Sb}_2\text{Te}_6$. The difference between the flux ratio and the estimated composition of the layers is attributed to the higher desorption rates of Sb and Te with respect to Ge at the deposition temperatures used. More details about the growth of GST by MBE can be found elsewhere.^{8,11–13} After the GST deposition, the samples were cooled down to room temperature and transferred to the *in-situ* magnetron sputtering chamber (base pressure: 5×10^{-8} mbar) for capping with W. For the sputtering of the 50 nm thick W contacting layer, an Ar pressure of 4.6×10^{-3} mbar, a 155 V DC bias, and RF power of 100 W were used. The resulting growth rate was approximately 8 nm/min. A schematic of the fabricated structure is shown in Fig. 1(a).

Structural characterization of the samples was performed by *in-situ* Reflection High Energy Electron Diffraction (RHEED), by X-Ray Diffraction (XRD) using a high resolution diffractometer (PANalytical X'PertTM) and by Scanning Electron Microscopy (SEM) (Hitachi S4800). Electrical tests were performed using an Agilent 81110 pulse generator to deliver fast programming pulses to the cell and a Keithley 236 parameter analyzer to take the readout of the programmed state in the DC regime, in an automatically switched AC/DC circuit. Dedicated pulse sequences are delivered to the cell in order to track the pulsed Current-Voltage (I-V) characteristic curves and the related Resistance-Current (R-I) programming curves for both the crystalline and amorphous states. In general, the collected characterizations aim at displaying the electrical properties of the grown chalcogenide material.

A typical RHEED pattern taken after the deposition of the GST layer is presented in Fig. 1(b). Clearly, diffraction rings can be observed, indicating that the deposited film is poly-crystalline. The polycrystalline nature of the film is confirmed by XRD and lattice spacings of 3.49 Å and 3.08 Å are obtained for the d_{111} and d_{002} , in good agreement with the lattice constant of epitaxial films grown under the same conditions. We note that for the deposition with the same growth parameters on crystalline substrates an epitaxial film is normally obtained. The formation of a poly-crystalline film is therefore attributed to the growth on the amorphous layers of the dedicated vehicle. Two representative SEM images of the sample surface after the deposition of the GST and W layers at different magnifications ((c) and (d)).

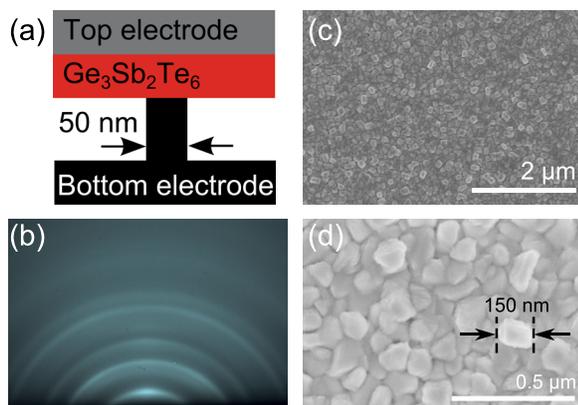


FIG. 1. Schematic of the device structure (a). RHEED pattern taken after the deposition of the GST layer (b). SEM images of the sample surface after the deposition of the GST and W layers at different magnifications ((c) and (d)).

images of the surface of the samples are shown in Figs. 1(c) and 1(d). They show that the surface is rough and grain like. From the SEM images, a grain size of 80–150 nm is determined. Since the initial starting surface was flat and the sputtered W films also are flat, the occurrence of the surface structure is attributed to the GST film. It is likely that this is caused by the dissimilar growth rates of grains with different orientations.

A very basic characterization of the grown material was performed using pulsed I-V measurements, in Fig. 2(a). For the virgin bit, a typical I-V curve of the crystalline state (SET, low resistance) is obtained, up to about $I = 1.7$ mA programming current, confirming the crystalline nature of the GST and the formation of a good contact with the electrodes. In order to obtain the I-V curve of the amorphous phase (RESET, high resistance), a RESET pulse was applied and the I-V characteristics were determined after a delay time of approximately 1 s. The curve related to the amorphous phase features the typical threshold voltage switching behavior at a voltage slightly below 1 V, as typically shown by PVD-deposited GST.¹⁴ Such behavior highlights the capability of MBE grown GST to be reversibly switched between two stable states, enabling the study of the threshold switching phenomenon in crystalline-grown materials. The magnification of the low-field region of the I-V curves, taken by more precise DC measurements, is reported in Fig. 2(b). By forcing increasing currents in the logarithmically spaced range between 10 nA and 100 μA and by measuring the resulting DC voltage drop on the device under test, a threshold voltage $V_{\text{TH}} = 0.85\text{--}0.9$ V can be precisely highlighted on the amorphous I-V curve. Moreover, the overall difference between the SET and RESET driven currents, evaluated at low-field or $V_{\text{READ}} = 0.1$ V, is a little more than 2 orders of magnitude, thus enabling large programming window operation and hence resulting in a large readout margin, as is required when handling large cell distributions.¹⁵

An important characteristic of a phase change memory device is the time it takes to switch between the phases in both the fast (write) and the slow (data-retention) regimes. Concerning the former, on one hand, it is known that in PCM the RESET operation is very fast and can be performed by a single pulse with a duration being in the range of a few tens of nanoseconds. The SET operation, on the other hand,

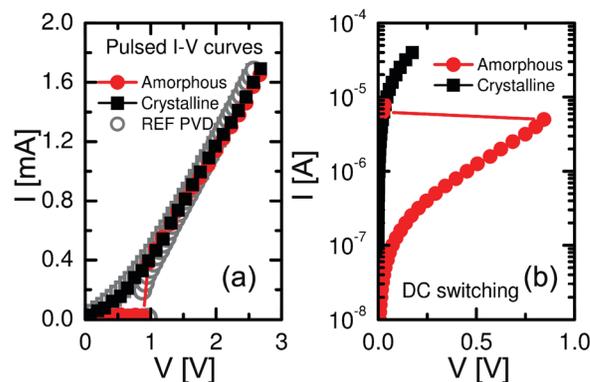


FIG. 2. Pulsed I-V characteristic curves and comparison with state of the art PVD GST in grey (a) and low-field DC I-V curves (b) of device with MBE GST.

is a little bit slower and electrical pulse widths in the 100 ns time range are typically required to anneal amorphous GST into its crystalline phase. This makes the SET operation more time-consuming and hence a speed limiting transition for the memory. In order to evaluate the SET performance of MBE grown GST, we performed R-I measurements in the RESET to SET transition by modulating on one hand the programming current amplitude and on the other hand the programming pulse duration applied to the cell, pre-conditioned in the RESET state before each programming pulse. This technique allows one to build up the electrical equivalent *Time-Temperature-Transformation* (e-TTT) surface, largely employed in optical data storage material exploration, in which the time variable is represented by the pulse duration; temperature is represented by the programming current and the transformation coordinate is here the logarithmic scale of resistance. This surface points out the performance of the SET operation, i.e., the minimum pulse duration, at optimum current amplitude, which is able to achieve the SET state. The measured e-TTT contour plot is shown in Fig. 3: data indicate that the SET state can be achieved with 0.7 mA electrical pulses with durations in the range between 150 and 200 ns, in full agreement with the SET performance expectations of state-of-the-art GST.¹⁶ This corresponds to an effective current density of approximately 3×10^{11} A/m². Further investigations of the SET performance in MBE grown GST will be the object of future work.

Concerning crystallization in the low temperature regime (data retention), the most representative parameters for material evaluation are the activation energy of crystallization, E_{Ax} , and the Arrhenius time pre-factor, τ_0 , extracted from the resistance-time curves taken at different temperature, here $T = 270^\circ\text{C}$, 290°C , and 300°C , as reported in Fig. 4. The application of the technique reported by Redaelli *et al.*¹⁷ allows the extraction of those parameters: we obtained an activation energy, $E_{Ax} = 2.6$ eV, as expected from GST and representing the energy barrier height to be overcome in the non-defective amorphous to crystal transition.¹⁸ As Arrhenius time pre-factor, we could extract $\tau_0 \approx 10^{-21}$ s that is 2–3 orders of magnitude higher than the value reported in the literature, highlighting a lower attempt

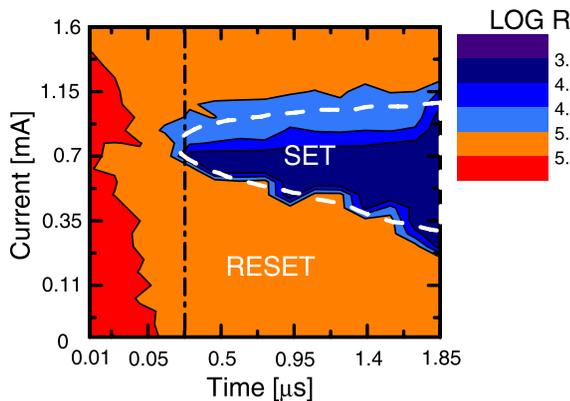


FIG. 3. e-TTT contour plot for the SET operation performance evaluation: it is worth noticing that a set pulse at optimum current around $800 \mu\text{A}$ enables reaching the SET state in $t_{\text{PULSE}} \approx 200$ ns or little less, in agreement with literature data.

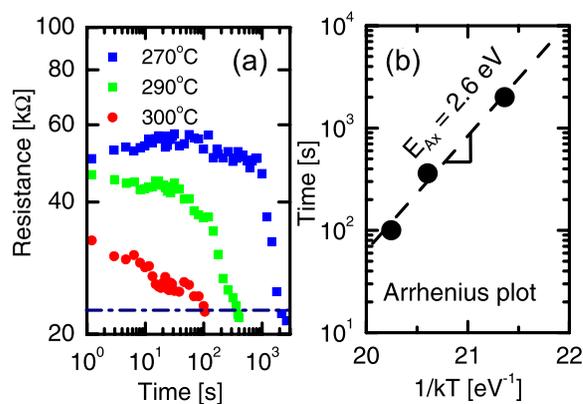


FIG. 4. Data retention characterization. Resistance vs. time plot taken at three different temperature (a) and Arrhenius plot of crystallization time (b).

frequency or decreased probability for overcoming the amorphous to crystalline energy barrier in MBE GST, with respect to PVD GST.

Another way of comparing materials with different alloys or fabrication process is through a resistance drift characterization. In fact, Structural Relaxation (SR) is known to be a typical phenomenon occurring in the amorphous phase of chalcogenide materials and it is widely reported to induce time-dependent phenomena impacting the electrical transport.¹⁹ Such phenomena are involved in the relaxation of defective configurations of bonds in the amorphous network and result in the resistance drift with time after programming in partially and fully amorphized cells due to thermal annealing of such defects, inducing the widening of the material energy gap.¹⁹ The resistance drift characteristic behavior against time of the MBE grown GST was evaluated in the whole programming window, in Fig. 5(a). The resistance-time curves show that the drift is very small in the SET state, increases with increasing resistance, and is maximum in the RESET state, at $R_{\text{RESET}} = 800$ k Ω . In particular, the drift power-law exponent extracted in a certain time interval has been reported to be the ratio between the shift of the activation energy of conduction and the shift of the activation energy of SR, within that time interval²⁰ and this entity therefore relates to the physical and structural parameters of the phase change material. For a more detailed analysis, the slopes in the resistance-time curves, represented by

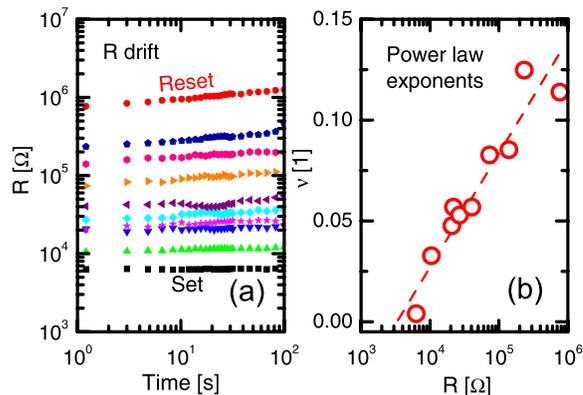


FIG. 5. Resistance drift characterization, including R-t plots in the entire programming window (a) and power law exponent plot as a function of resistance (b).

their power-law exponents,²⁰ are reported in Fig. 5(b) as a function of the initial resistance states, measured at about 1 s after pulse. The power-law exponents range from $\nu < 0.01$ at SET to $\nu = 0.11$ – 0.12 at RESET and are in good agreement with literature values.²⁰ Thus, Fig. 5 delivers further evidence that an amorphous GST, quenched from a MBE grown GST, is in good alignment to the state of the art PVD deposited GST, from the structural relaxation and transport properties standpoint.

In summary, a MBE grown polycrystalline GST alloy has been integrated in a PCM testing vehicle allowing for electrical characterizations. I-V curves of the device displayed a $V_{TH} = 0.85$ – 0.9 V and revealed that a programming window larger than 2 orders of magnitude could be obtained. Intrinsic material properties, such as structural relaxation and crystallization activation energy, were analyzed and found to be in agreement with the previous studies. Furthermore, it was demonstrated that the SET state could be obtained with 200 ns long electrical pulses. The material characterization thus indicates a very good alignment between the MBE and PVD GST. Based on these results and by taking into account that a high degree of material purity and compositional control can be achieved by using MBE, it is concluded that MBE is an intrinsically well suited deposition technique for chalcogenide materials for phase change memory.

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